ABSTRACT

The objective of the present invention is to provide a data transfer control device that enables a reduction in the processing load on the firmware during the occurrence of a bus reset, and electronic equipment using the same. A data transfer control device in accordance with the IEEE 1394 standard generates a bit BT that toggles whenever one received packet and the next received packet are received in different bus reset intervals, and comprises that BT in the header of each packet stored in RAM. Bus reset pointers (a bus reset header pointer and a bus reset ORB pointer) that indicate a bus reset boundary in RAM are provided, enabling simple differentiation between a packet received before a bus reset occurred and a packet received after the reset. If transmission has been halted by the occurrence of the bus reset, the bus reset transmission halt status is passed to the firmware via a register.